EE 671: VLSI DESIGN 2025-2026

Project 1: Standard Cell Library Characterization and Design

Team Number: 04

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Contents

1 Project Overview **3**
1.1 Introduction . . . 3
1.2 Project Objectives . . . 3

2 Cell 1: BUF (Buffer) **4**
2.1 Cell Summary . . . 4
2.2 Circuit Diagram . . . 4
2.3 MOSFET Width and Length . . . 5
2.4 Layout . . . 5
2.5 PEX Netlist (screenshot / excerpt) . . . 6
2.6 DRC and LVS . . . 6
2.7 Simulation Waveforms . . . 7
2.8 Timing and Power Characterization . . . 8
2.8.1 Input Pin Capacitances . . . 8
2.8.2 Transition Times . . . 8
2.8.3 Propagation Delay Times . . . 8
2.8.4 Static Power . . . 9
2.8.5 Dynamic Power . . . 9

3 Cell 2: DF-XTP (Delay Flip-Flop, posedge CLK, single output Q) **10**
3.1 Cell Summary . . . 10
3.2 Circuit Diagram . . . 10
3.3 MOSFET Width and Length . . . 11
3.4 Layout . . . 11
3.5 PEX Netlist . . . 12
3.6 DRC and LVS . . . 13
3.7 Simulation Waveforms . . . 14
3.8 Timing and Power Characterization — DF-XTP . . . 15
3.8.1 Input Pin Capacitances . . . 15
3.8.2 Setup Time Constraints . . . 15
3.8.3 Hold Time Constraints . . . 15
3.8.4 Transition Times . . . 16
3.8.5 CLK-to-Q Delay Times . . . 16
3.8.6 Static Power . . . 16
3.8.7 Dynamic Power . . . 17

4 Cell 3: AND2B (2-input AND, first input inverted) 18
4.1 Cell Summary . . . 18
4.2 Circuit Diagram . . . 18
4.3 MOSFET Width and Length . . . 19
4.4 Layout . . . 19
4.5 PEX Netlist . . . 20
4.6 DRC and LVS . . . 20
4.7 Simulation Waveforms . . . 21
4.8 Timing and Power Characterization — AND2B . . . 22
4.8.1 Transition Times . . . 22
4.8.2 Propagation Delay Times . . . 23
4.8.3 Static Power . . . 24
4.8.4 Dynamic Power . . . 24

5 Team Contributions 26

6 References 27

Chapter 1

Project Overview

1.1 Introduction

This project involves the characterization and design of three standard cells in the standard-cell library (all strength-1): `BUF` (buffer), `DF-XTP` (delay flop, single output Q, posedge clk), and `AND2B` (2-input AND, first input inverted). For each cell we provide circuit diagrams, MOS sizes, layout screenshots, PEX netlist screenshots, DRC/LVS results, simulation waveforms, and timing/power characterization tables as required by the course specification.

1.2 Project Objectives

- Design NGSpice circuit for each cell with rise/fall similar to inverter 1x.
- Draw layout in Magic and ensure zero DRC errors and LVS pass.
- Extract LEF, PEX netlists, perform timing, power and input cap characterization.
- Provide a Verilog functional view and verify with Icarus Verilog.

Chapter 2

Cell 1: BUF (Buffer)

2.1 Cell Summary

Cell name: `BUF`
Cell type: Combinational (Buffer)
VDD used for all simulations: `1.8 V`

2.2 Circuit Diagram

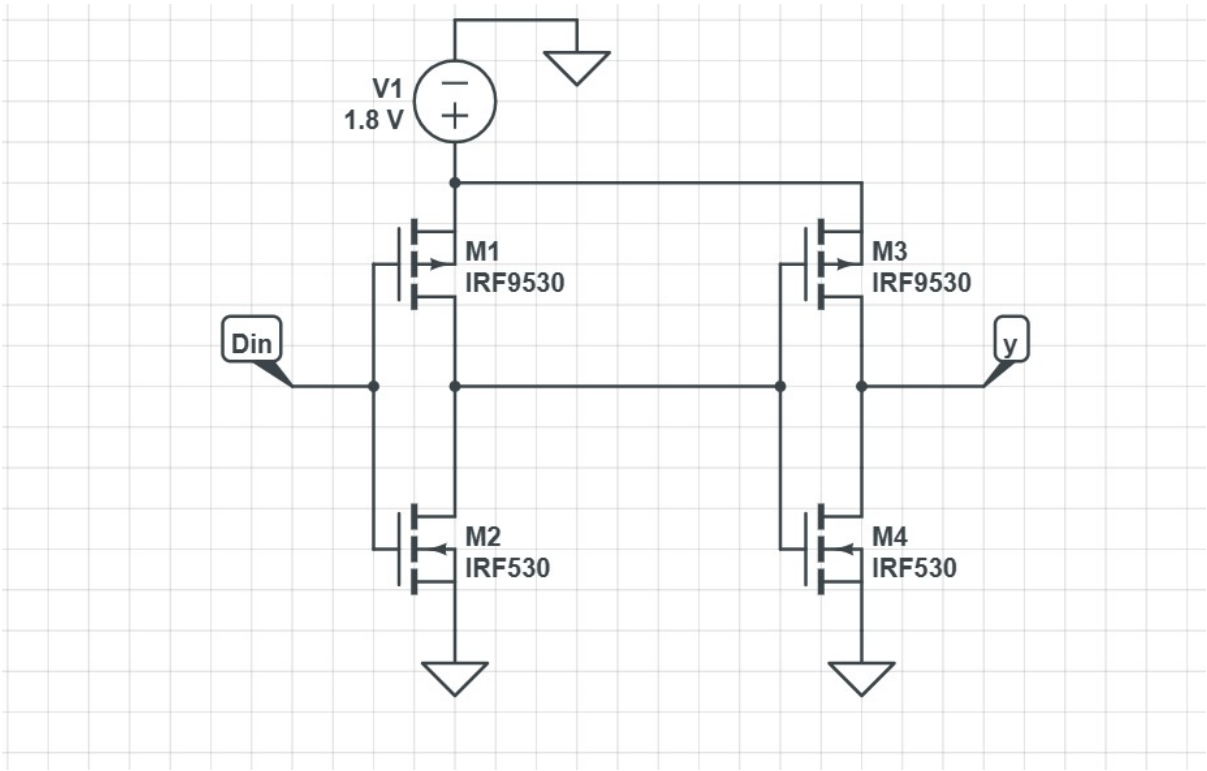

Figure 2.1: Circuit diagram of BUF.

2.3 MOSFET Width and Length

Table 2.1: MOSFET Width and Length for BUF (as used in the design)

Device	Type	Width (µm)	Length (µm)
M1	NMOS	0.49	0.15
M2	PMOS	1.46	0.15

2.4 Layout

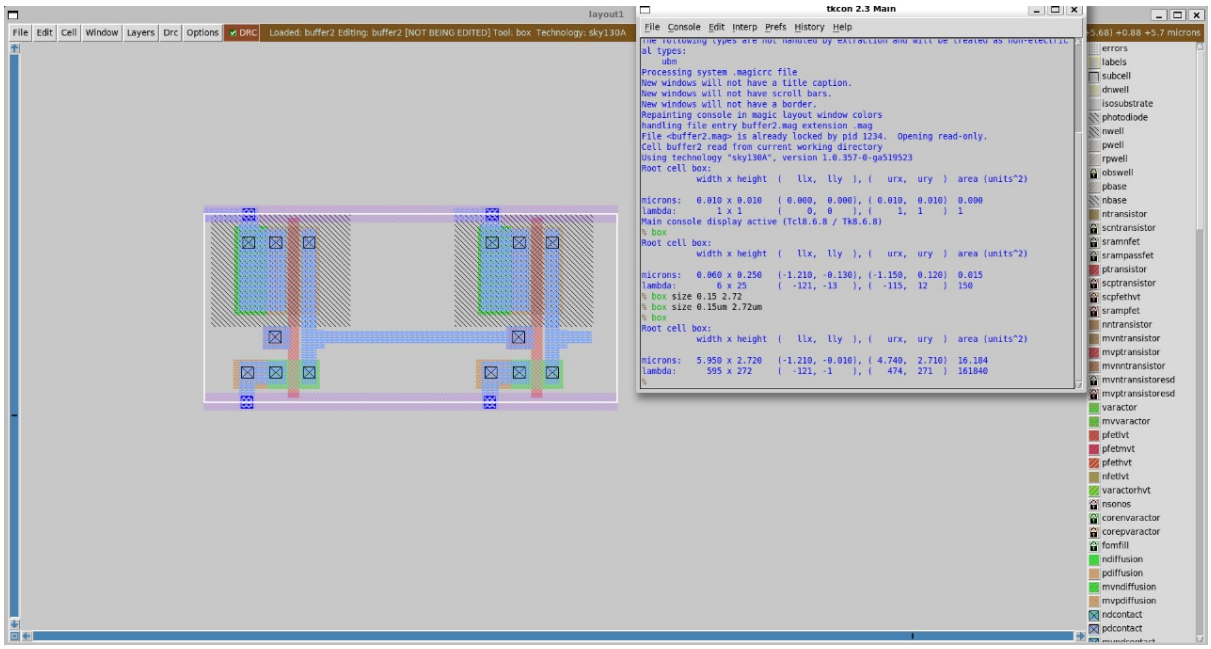

Figure 2.2: BUF layout. (Width x Height: __ µm x __ µm)

2.5 PEX Netlist (screenshot / excerpt)

```
* NGSPICE file created from buffer2.ext - technology: sky130A

X0 a_15_18# in vdd vdd sky130_fd_pr__pfet_01v8 ad=0.378 pd=3.12 as=0.378 ps=3.12 w=1.26 l=0.15
X1 out a_15_18# Vss Vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.44 w=0.42 l=0.15
X2 out a_15_18# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.378 pd=3.12 as=0.378 ps=3.12 w=1.26 l=0.15
X3 a_15_18# in Vss Vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.44 w=0.42 l=0.15
C0 out vdd 0.12461f
C1 in a_15_18# 0.05634f
C2 vdd a_15_18# 0.22925f
C3 in vdd 0.04886f
C4 out a_15_18# 0.05361f
C5 out Vss 0.17466f
C6 in Vss 0.22793f
C7 vdd Vss 1.38852f
C8 a_15_18# Vss 0.55718f
```

Figure 2.3: PEX netlist screenshot for BUF.

2.6 DRC and LVS

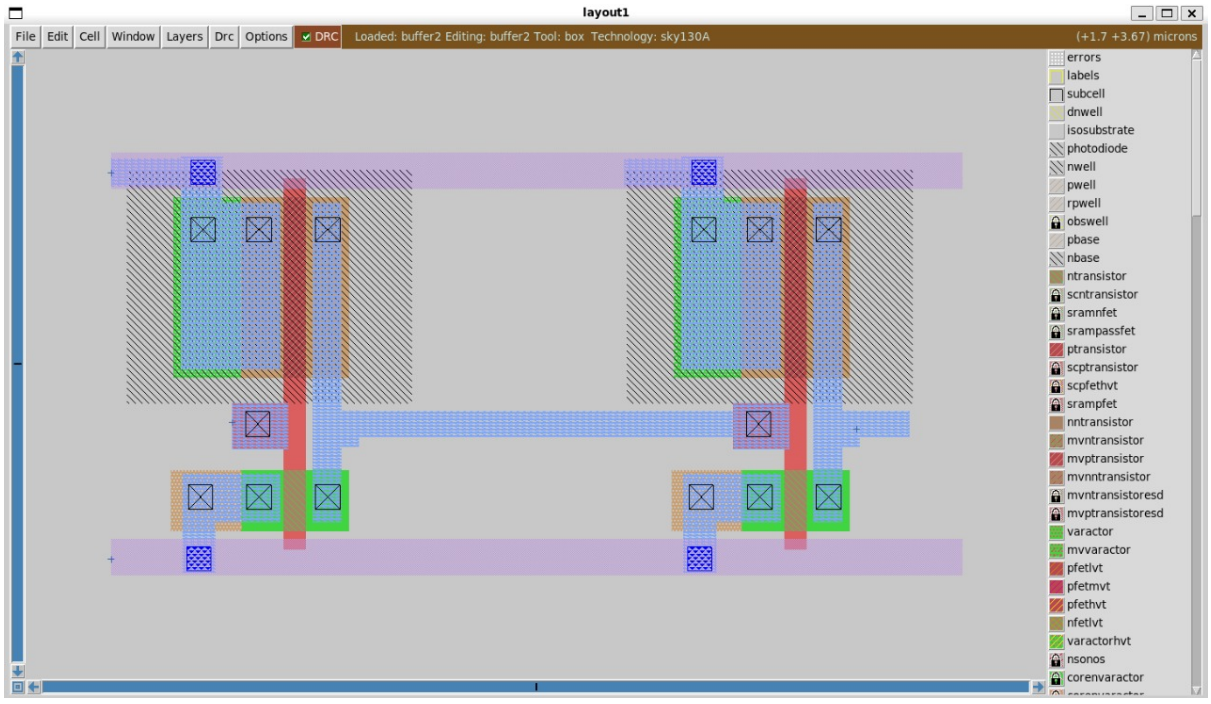

Figure 2.4: DRC clean screenshot for BUF.

```
Contents of circuit 1:  Circuit: 'buffer2'
Circuit buffer2 contains 4 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 5 nets.
Contents of circuit 2:  Circuit: 'buffer2'
Circuit buffer2 contains 4 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   2
  Class: sky130_fd_pr__pfet_01v8 instances:   2
Circuit contains 5 nets.

Circuit 1 contains 4 devices, Circuit 2 contains 4 devices.
Circuit 1 contains 5 nets,    Circuit 2 contains 5 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

Figure 2.5: LVS clean screenshot for BUF.

2.7 Simulation Waveforms

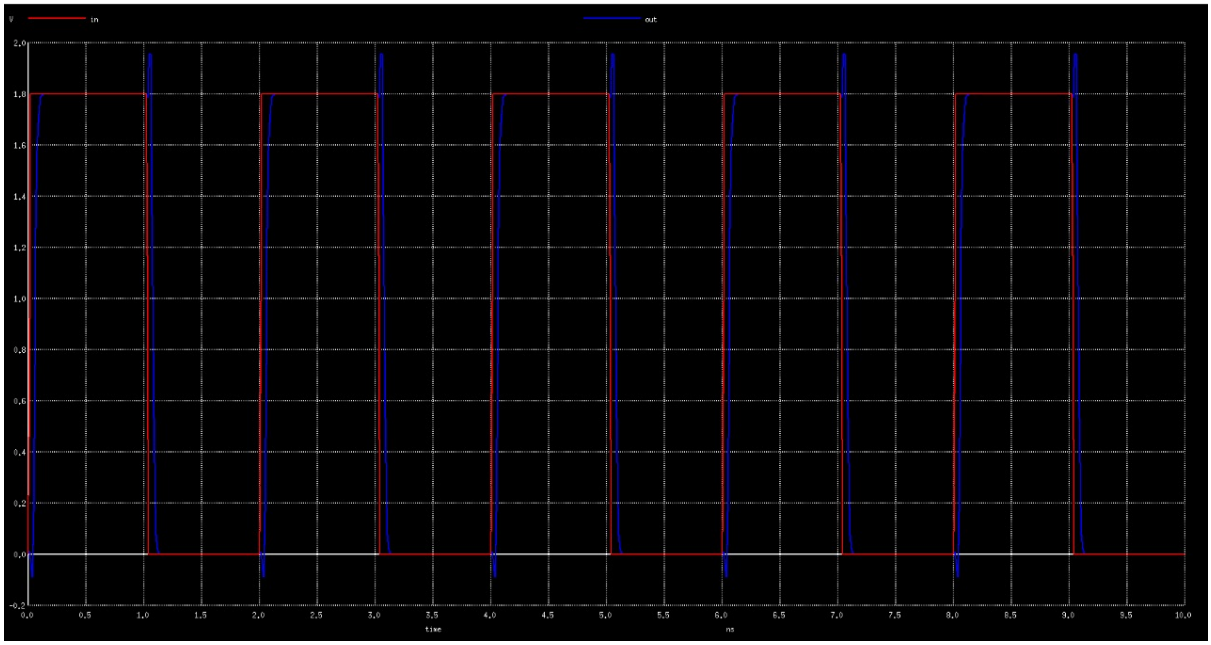

Figure 2.6: Waveform used for measurement (inputs, outputs). Mark measurement cursors on this plot.

2.8 Timing and Power Characterization

The following tables are filled from the provided extraction/simulation data (source: uploaded `buf.docx`). :contentReference[oaicite:0]index=0

2.8.1 Input Pin Capacitances

Table 2.2: Input pin capacitances for BUF (pF)

Input Pin	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
A	0.00240	0.00181	0.00211

2.8.2 Transition Times

Output Rise Transitions (ns) — Related pin A (other pins held constant):

Table 2.3: Output Rise Transitions (20%–80%) — BUF (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0149	0.0681	0.598
100 ps	0.0150	0.0681	0.598
1000 ps	0.0304	0.0745	0.599

Output Fall Transitions (ns) — Related pin A:

Table 2.4: Output Fall Transitions (20%–80%) — BUF (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0148	0.0729	0.641
100 ps	0.0150	0.0729	0.641
1000 ps	0.0281	0.0796	0.643

2.8.3 Propagation Delay Times

(Definition used: 50% input to 50% output)

Cell Rise Delay (ns) — Related pin A:

Table 2.5: Cell Rise Delay (50%–50%) — BUF (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0480	0.0891	0.451
100 ps	0.0666	0.108	0.470
1000 ps	0.148	0.200	0.563

Cell Fall Delay (ns) — Related pin A:

Table 2.6: Cell Fall Delay (50%–50%) — BUF (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0471	0.0970	0.531
100 ps	0.0687	0.119	0.554
1000 ps	0.161	0.221	0.660

2.8.4 Static Power

Table 2.7: Static Power for BUF (nW)

Input Condition (A)	Power (nW)
0	0.112
1	0.112

2.8.5 Dynamic Power

Rise Power (nW) — Related pin A:

Table 2.8: Rise Power (nW) — BUF

Input Slew	0.5 fF	10 fF	100 fF
10 ps	211159	306101	327084
100 ps	207950	304687	327320
1000 ps	113913	289849	326025

Fall Power (nW) — Related pin A:

Table 2.9: Fall Power (nW) — BUF

Input Slew	0.5 fF	10 fF	100 fF
10 ps	166846	28706	2830
100 ps	168246	26932	2829
1000 ps	100931	39376	1437

Chapter 3

Cell 2: DF-XTP (Delay Flip-Flop, posedge CLK, single output Q)

3.1 Cell Summary

Cell name: `DFXTP`
Cell type: Sequential (Positive-edge triggered D flip-flop)
VDD used: `1.8 V`

3.2 Circuit Diagram

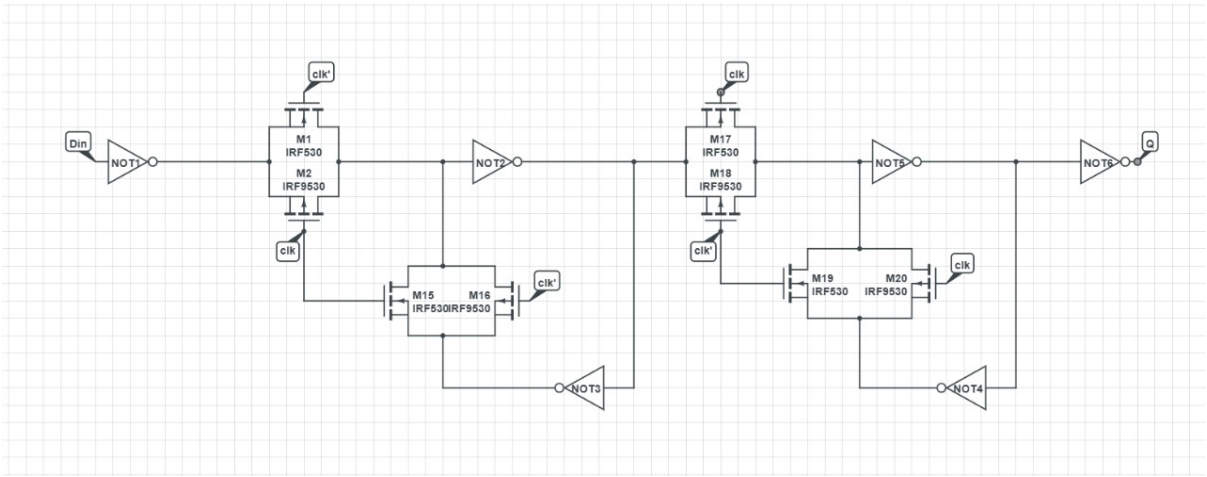

Figure 3.1: Circuit diagram of DF-XTP.

3.3 MOSFET Width and Length

Table 3.1: MOSFET Width and Length for DF-XTP

Device	Type	Width (µm)	Length (µm)
xm01	PMOS	1.28	0.15
xm02	NMOS	0.42	0.15
xm01	PMOS	1.28	0.15
xm02	NMOS	0.42	0.15

3.4 Layout

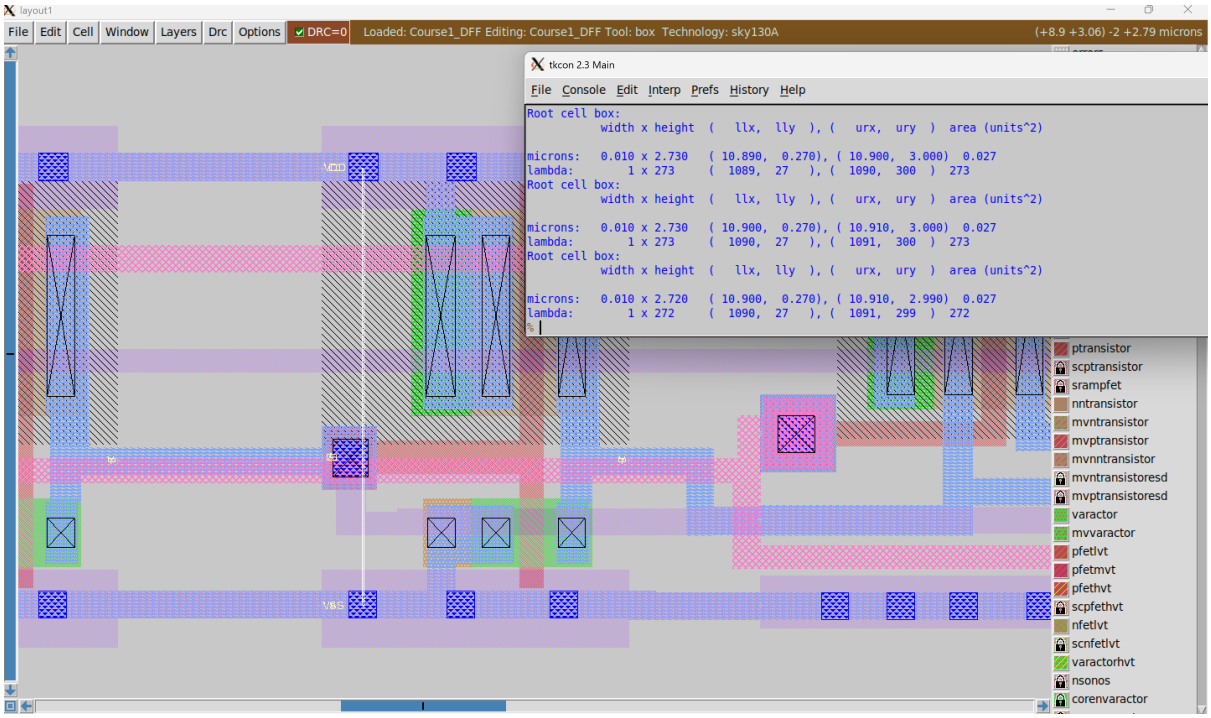

Figure 3.2: DF-XTP layout (Width x Height: __ µm x __ µm).

3.5 PEX Netlist

```
* NGSPICE file created from Course1_DFF.ext - technology: sky130A
.lib /home/manjima/pdk/open_pdks/sky130/sky130A/libs.tech/ngspice/sky130.lib.spice tt
VSS0 VSS 0 DC 0
VDD VDD VSS DC 1.8
Vin D VSS pulse(0 1.8 1n 20p 20p 4n 8n)

V1 clk VSS pulse(0 1.8 0 20p 20p 2n 4n)

.subckt Course1_inv A VDD VSS Y
X0 Y A VSS VSS sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X1 Y A VDD VDD sky130_fd_pr__pfet_01v8 ad=0.4212 pd=3.22 as=0.384 ps=3.16 w=1.28 l=0.15
**devattr s=3840,316 d=4212,322
C0 Y VDD 0.1351f
C1 VDD A 0.15318f
C2 Y A 0.03408f
C3 Y VSS 0.16239f
C4 A VSS 0.31592f
C5 VDD VSS 0.7053f
.ends

.subckt Course1_tg A clk_bar clk VDD VSS Y
X0 Y clk A VSS sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
X1 Y clk_bar A VDD sky130_fd_pr__pfet_01v8 ad=0.384 pd=3.16 as=0.384 ps=3.16 w=1.28 l=0.15
**devattr s=3840,316 d=3840,316
C0 Y VDD 0.08342f
C1 A VDD 0.15963f
C2 A Y 0.20029f
C3 VDD clk_bar 0.11834f
C4 Y clk_bar 0.00718f
C5 A clk_bar 0.07841f
C6 VDD clk 0.00399f
C7 Y clk 0.08707f
C8 A clk 0.00805f
C9 clk clk_bar 0.00166f
C10 clk VSS 0.38469f
C11 Y VSS 0.22689f
C12 A VSS 0.24226f
C13 clk_bar VSS 0.26553f
C14 VDD VSS 0.9093f
.ends
xD1 D clk vdd gnd Q Course1_DFF
.subckt Course1_DFF D clk VDD VSS Q
XCourse1_inv_0 D VDD VSS Course1_tg_0/A Course1_inv
XCourse1_inv_1 Course1_tg_1/Y VDD VSS Course1_tg_2/A Course1_inv
XCourse1_inv_2 Course1_tg_2/A VDD VSS Course1_tg_1/A Course1_inv
XCourse1_inv_3 Course1_tg_3/Y VDD VSS Course1_inv_5/A Course1_inv
XCourse1_inv_4 Course1_inv_5/A VDD VSS Course1_tg_3/A Course1_inv
XCourse1_inv_5 Course1_inv_5/A VDD VSS Q Course1_inv
XCourse1_inv_6 clk VDD VSS Course1_inv_6/Y Course1_inv
XCourse1_tg_0 Course1_tg_0/A clk Course1_inv_6/Y VDD VSS Course1_tg_1/Y Course1_tg
XCourse1_tg_1 Course1_tg_1/A Course1_inv_6/Y clk VDD VSS Course1_tg_1/Y Course1_tg
XCourse1_tg_3 Course1_tg_3/A clk Course1_inv_6/Y VDD VSS Course1_tg_3/Y Course1_tg
XCourse1_tg_2 Course1_tg_2/A Course1_inv_6/Y clk VDD VSS Course1_tg_3/Y Course1_tg
C0 VDD Course1_inv_6/Y 0.1811f
C1 clk Course1_tg_2/A 0.12448f
C2 VSS VDD -0.32878f
C3 Course1_inv_5/A Course1_tg_2/A 0.00209f
C4 Course1_tg_0/A clk 0.07212f
C5 Course1_tg_1/Y VDD 0.58628f
C6 VDD D 0.00271f
C7 clk Course1_tg_1/A 0.02981f
C8 VDD Course1_tg_3/Y 0.57421f
C9 Q clk 0
```

Figure 3.3: PEX netlist screenshot for DF-XTP - 1.

```
C7 clk Course1_tg_1/A 0.02981f
C8 VDD Course1_tg_3/Y 0.57421f
C9 Q clk 0
C10 clk Course1_inv_6/Y 1.40536f
C11 Course1_tg_0/A Course1_tg_2/A 0
C12 VSS clk 0.08209f
C13 Q Course1_inv_5/A 0.00267f
C14 Course1_inv_5/A Course1_inv_6/Y 0.39285f
C15 Course1_tg_2/A Course1_tg_1/A 0.13202f
C16 VSS Course1_inv_5/A 1.00133f
C17 Course1_tg_1/Y clk 0.20411f
C18 clk D 0.02482f
C19 Course1_inv_6/Y Course1_tg_2/A 0.46412f
C20 Course1_inv_5/A Course1_tg_1/Y 0
C21 VSS Course1_tg_2/A 0.83774f
C22 clk Course1_tg_3/Y 0.30173f
C23 Course1_tg_0/A Course1_inv_6/Y 0.04453f
C24 Course1_inv_5/A Course1_tg_3/Y 0.36651f
C25 VSS Course1_tg_0/A 0.04417f
C26 Course1_tg_1/Y Course1_tg_2/A 0.32303f
C27 Course1_inv_6/Y Course1_tg_1/A 0.06821f
C28 VSS Course1_tg_1/A -0.00281f
C29 Course1_tg_0/A Course1_tg_1/Y 0
C30 Q Course1_inv_6/Y 0.00113f
C31 Course1_tg_3/Y Course1_tg_2/A 0
C32 Course1_tg_0/A D 0.00113f
C33 VSS Course1_inv_6/Y 1.14951f
C34 Course1_tg_1/Y Course1_tg_1/A 0.06955f
C35 Course1_tg_3/A VDD 0.02246f
C36 Course1_tg_1/Y Course1_inv_6/Y 0.21702f
C37 Course1_inv_6/Y D 0.02954f
C38 VSS Course1_tg_1/Y 0.11957f
C39 VSS D 0
C40 Q Course1_tg_3/Y 0
C41 Course1_tg_3/Y Course1_inv_6/Y 0.08082f
C42 VSS Course1_tg_3/Y 0.08812f
C43 Course1_tg_1/Y D 0
C44 Course1_tg_3/A clk 0.04776f
C45 Course1_tg_1/Y Course1_tg_3/Y 0.0029f
C46 Course1_inv_5/A Course1_tg_3/A 0.1305f
C47 clk VDD 0.98673f
C48 Course1_inv_5/A VDD 0.07975f
C49 Course1_tg_3/A Course1_inv_6/Y 0.03775f
C50 VSS Course1_tg_3/A 0.00974f
C51 VDD Course1_tg_2/A 0.07429f
C52 Course1_tg_0/A VDD 0.02932f
C53 Course1_tg_3/A Course1_tg_3/Y 0.07437f
C54 Course1_inv_5/A clk 0.0935f
C55 VDD Course1_tg_1/A 0.02085f
C56 VSS 0 0.52987f
C57 VDD 0 9.18774f
C58 Course1_tg_3/Y 0 0.87863f
C59 Course1_tg_1/Y 0 0.90667f
C60 Course1_inv_6/Y 0 3.02373f
C61 clk 0 3.12733f
C62 Q 0 0.15946f
C63 Course1_tg_3/A 0 0.40187f
C64 Course1_inv_5/A 0 0.93374f
C65 Course1_tg_1/A 0 0.38356f
C66 Course1_tg_2/A 0 0.81938f
C67 Course1_tg_0/A 0 0.38244f
C68 D 0 0.29239f
.ends

.control
tran 0.1ps 50ns
set xbrushwidth=2
.ends
```

Figure 3.4: PEX netlist screenshot for DF-XTP - 2.

3.6 DRC and LVS

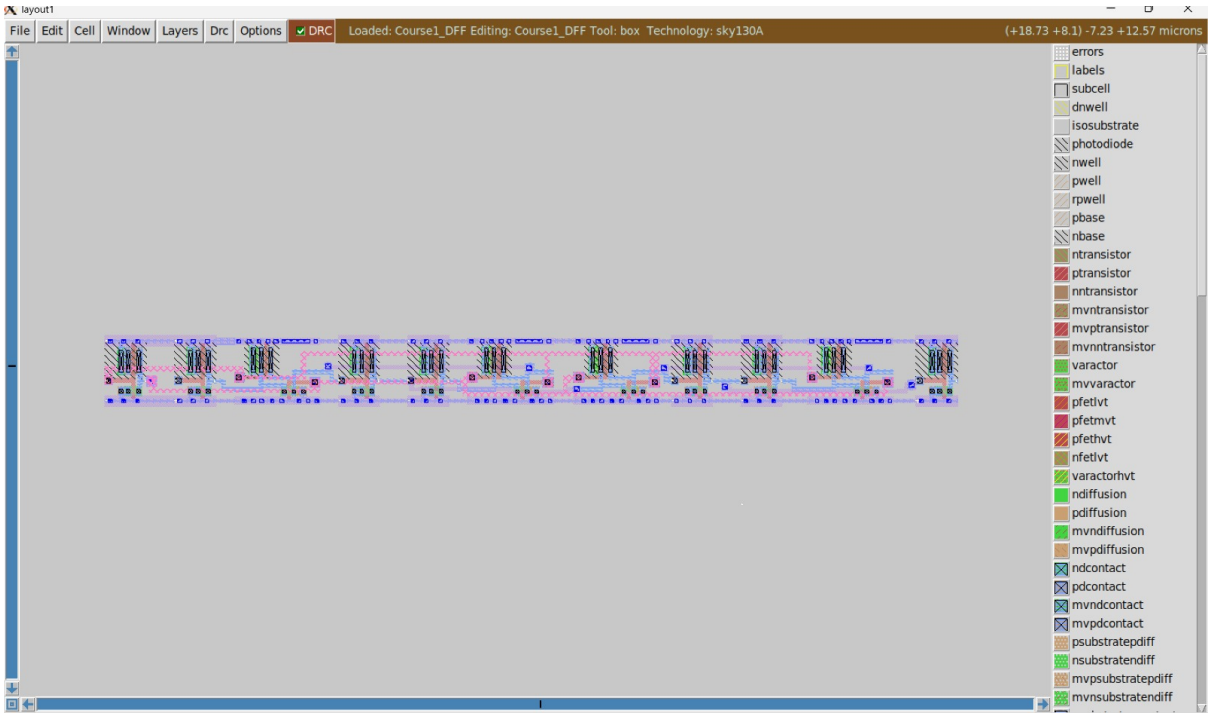

Figure 3.5: DRC clean screenshot for DF-XTP.

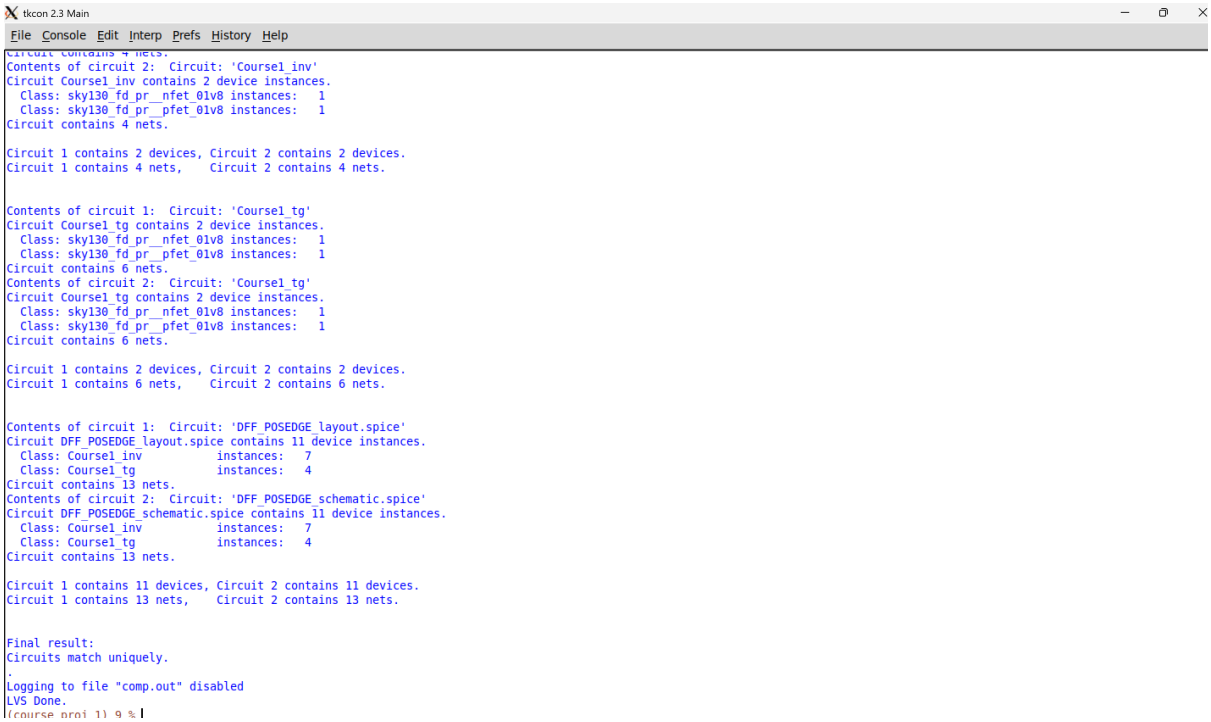

Figure 3.6: LVS clean screenshot for DF-XTP.

3.7 Simulation Waveforms

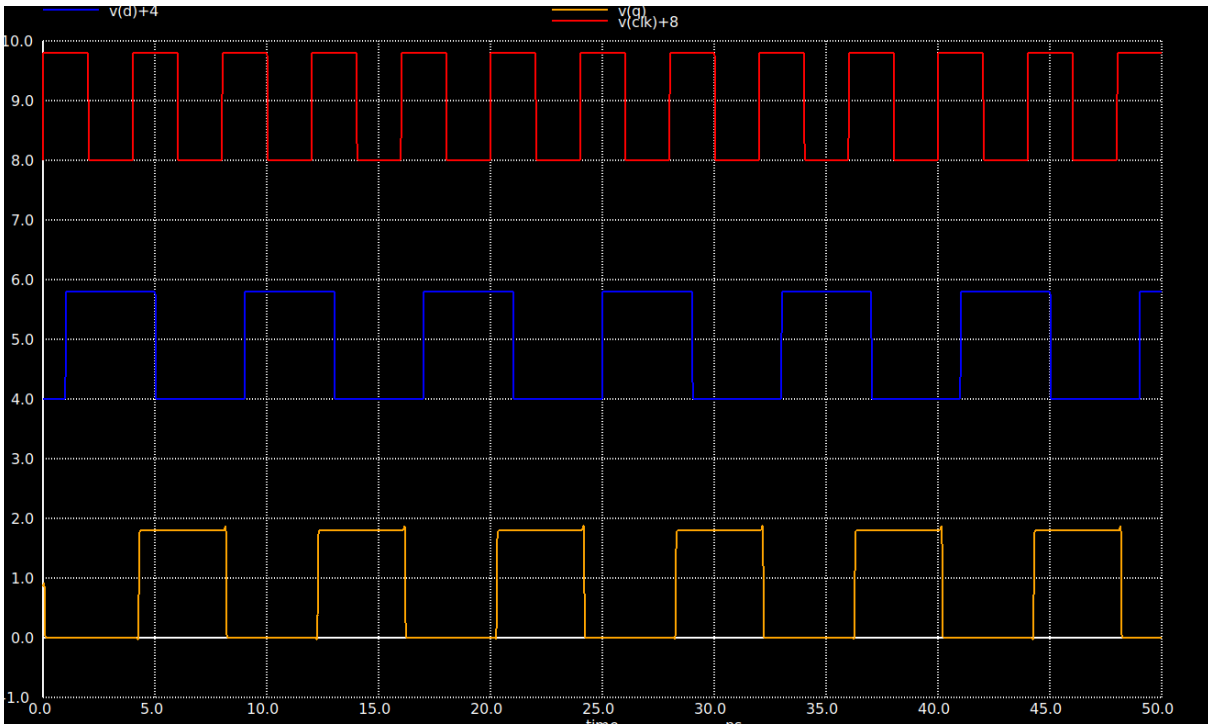

Figure 3.7: Setup time waveform (show D and CLK, and cursor markers).

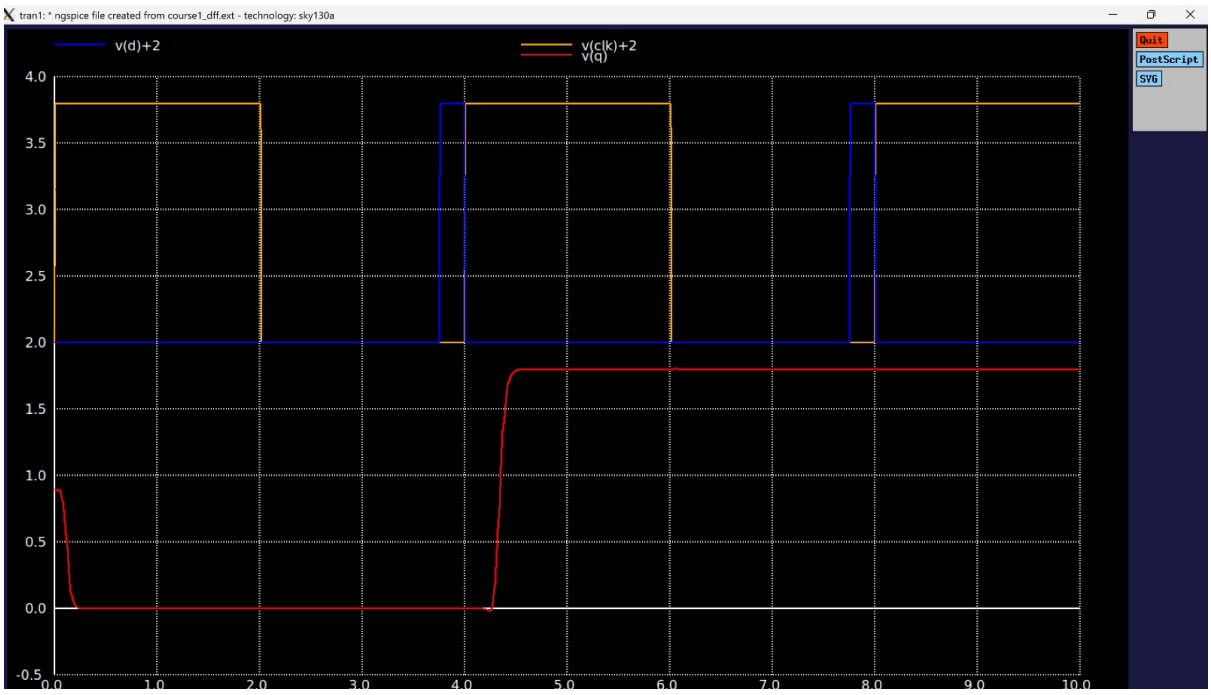

Figure 3.8: Hold time waveform (show D and CLK, and cursor markers).

3.8 Timing and Power Characterization — DF-XTP

3.8.1 Input Pin Capacitances

Table 3.2: Input pin capacitances for D Flip-Flop (pF)

Input Pin	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
D	0.00299149	0.002984402	0.002987946
CLK	0.0158483	0.01644586	0.01614708

3.8.2 Setup Time Constraints

Rise Constraint (ns) [Input slew vs CLK slew]

Table 3.3: Setup Time Rise Constraint (ns)

Input Slew	10 ps	1000 ps
10 ps	0.150	0
1000 ps	0.83	0.160

Fall Constraint (ns) [Input slew vs CLK slew]

Table 3.4: Setup Time Fall Constraint (ns)

Input Slew	10 ps	1000 ps
10 ps	0.150	0
1000 ps	0.83	0.160

3.8.3 Hold Time Constraints

Rise Constraint (ns) [Input slew vs CLK slew]

Table 3.5: Hold Time Rise Constraint (ns)

Input Slew	10 ps	1000 ps
10 ps	0.190	0
1000 ps	0.650	0.275

Fall Constraint (ns) [Input slew vs CLK slew]

Table 3.6: Hold Time Fall Constraint (ns)

Input Slew	10 ps	1000 ps
10 ps	0.190	0
1000 ps	0.650	0.275

3.8.4 Transition Times

Output Rise Transitions (ns) — Related pin D

Table 3.7: Output Rise Transitions — Related pin D (ns)

Output Capacitance	10 ps	100 ps	1000 ps
0.5 fF	0.028898	0.028898	0.028112
10 fF	0.075968	0.075968	0.075886
100 fF	0.587585	0.587598	0.642442

Output Fall Transitions (ns) — Related pin D

Table 3.8: Output Fall Transitions — Related pin D (ns)

Output Capacitance	10 ps	100 ps	1000 ps
0.5 fF	0.024464	0.024464	0.024464
10 fF	0.08031	0.08031	0.08031
100 fF	0.642435	0.642442	0.587576

3.8.5 CLK-to-Q Delay Times

Cell Rise Delay (ns) — Related pin D

Table 3.9: Cell Rise Delay — Related pin D (ns)

Output Capacitance	10 ps	100 ps	1000 ps
0.5 fF	0.279141	0.297403	0.4804
10 fF	0.330395	0.34866	0.531583
100 fF	0.6873	0.705574	0.88516

Cell Fall Delay (ns) — Related pin D

Table 3.10: Cell Fall Delay — Related pin D (ns)

Output Capacitance	10 ps	100 ps	1000 ps
0.5 fF	0.190366	0.208233	0.353954
10 fF	0.249099	0.266976	0.413345
100 fF	0.68726	0.705148	0.851856

3.8.6 Static Power

Table 3.11: Static Power for D Flip-Flop (nW)

Condition (CLK,D)	Power (nW)
00	68949.72
01	0.3945
10	114916
11	0.5087682

3.8.7 Dynamic Power

Rise Power (nW) — Related pin D

Table 3.12: Rise Power — D Flip-Flop (nW)

Output Capacitance	10 ps	100 ps	1000 ps
0.5 fF	231729	231743	235276
10 fF	232030	235105	249413
100 fF	332147	295043	294238

Fall Power (nW) — Related pin D

Table 3.13: Fall Power — D Flip-Flop (nW)

Output Capacitance	10 ps	100 ps	1000 ps
0.5 fF	283121	284043	276583
10 fF	111864	112336	415084
100 fF	23761.9	21919.5	25543.9

Chapter 4

Cell 3: AND2B (2-input AND, first input inverted)

4.1 Cell Summary

Cell name: `AND2B`
Cell type: Combinational (2-input AND where input A is inverted before the AND)
VDD used: `1.8 V`

4.2 Circuit Diagram

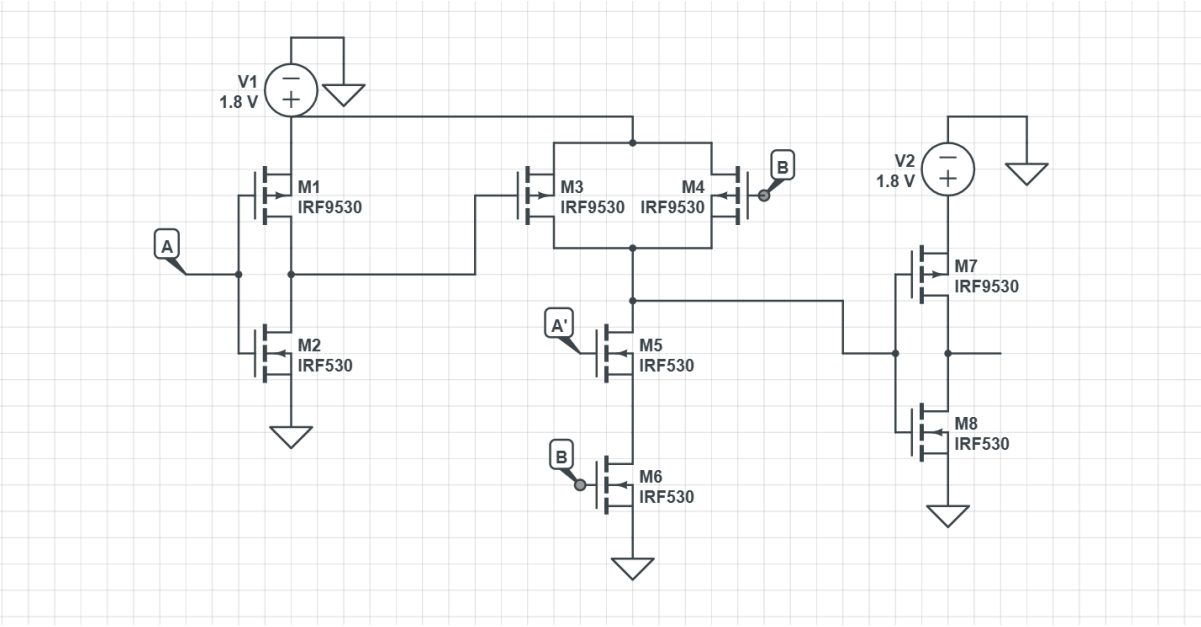

Figure 4.1: Circuit diagram of AND2B.

4.3 MOSFET Width and Length

Table 4.1: MOSFET Width and Length for AND2B

Device	Type	Width (µm)	Length (µm)
M1 (not1)	PMOS	1.26	0.15
M2 (not1)	NMOS	0.42	0.15
M1 (nand)	PMOS	0.84	0.15
M2 (nand)	PMOS	0.84	0.15
M3 (nand)	NMOS	0.84	0.15
M4 (nand)	NMOS	0.84	0.15
M1 (inv)	PMOS	1.26	0.15
M2 (inv)	NMOS	0.42	0.15

4.4 Layout

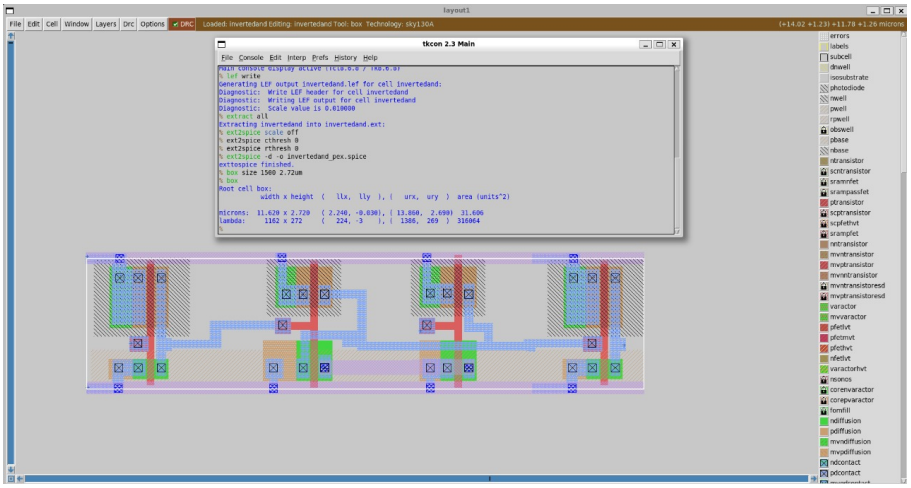

Figure 4.2: AND2B layout (Width x Height: __ µm x __ µm).

4.5 PEX Netlist

```
* SPICE3 file created from invertedand.ext - technology: sky130A

X0 a_661_14# a_365_18# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.252 pd=2.28 as=0.252 ps=2.16 w=0.84 l=0.15
X1 a_661_14# B vdd vdd sky130_fd_pr__pfet_01v8 ad=0.252 pd=2.28 as=0.252 ps=2.16 w=0.84 l=0.15
X2 a_365_18# A vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.29 w=0.42 l=0.15
X3 out a_661_14# vss vss sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps=1.29 w=0.42 l=0.15
X4 a_365_18# A vdd vdd sky130_fd_pr__pfet_01v8 ad=0.378 pd=3.12 as=0.378 ps=3.24 w=1.26 l=0.15
X5 out a_661_14# vdd vdd sky130_fd_pr__pfet_01v8 ad=0.378 pd=3.12 as=0.378 ps=3.24 w=1.26 l=0.15
X6 a_706_14# a_365_18# a_661_14# vss sky130_fd_pr__nfet_01v8 ad=0.252 pd=2.28 as=0.252 ps=2.28 w=0.84 l=0.15
X7 a_706_14# B vss vss sky130_fd_pr__nfet_01v8 ad=0.252 pd=2.28 as=0.252 ps=2.58 w=0.84 l=0.15
C0 B a_661_14# 0.08378f
C1 a_706_14# A 0
C2 vdd a_365_18# 0.18927f
C3 a_706_14# a_661_14# 0.14829f
C4 out a_661_14# 0.05236f
C5 B vdd 0.04561f
C6 vdd a_706_14# 0.07573f
C7 B a_365_18# 0.00598f
C8 a_706_14# a_365_18# 0.00568f
C9 vdd out 0.1159f
C10 a_365_18# out 0
C11 B a_706_14# 0.01463f
C12 A a_661_14# 0
C13 B out 0
C14 a_706_14# out 0
C15 vdd A 0.04887f
C16 vdd a_661_14# 0.26872f
C17 A a_365_18# 0.05424f
C18 a_365_18# a_661_14# 0.05568f
C19 out vss 0.14961f
C20 B vss 0.24799f
C21 A vss 0.23046f
C22 vdd vss 2.27435f
C23 a_706_14# vss 0.56595f
C24 a_661_14# vss 0.84651f
C25 a_365_18# vss 0.5727f
```

Figure 4.3: PEX netlist screenshot for AND2B.

4.6 DRC and LVS

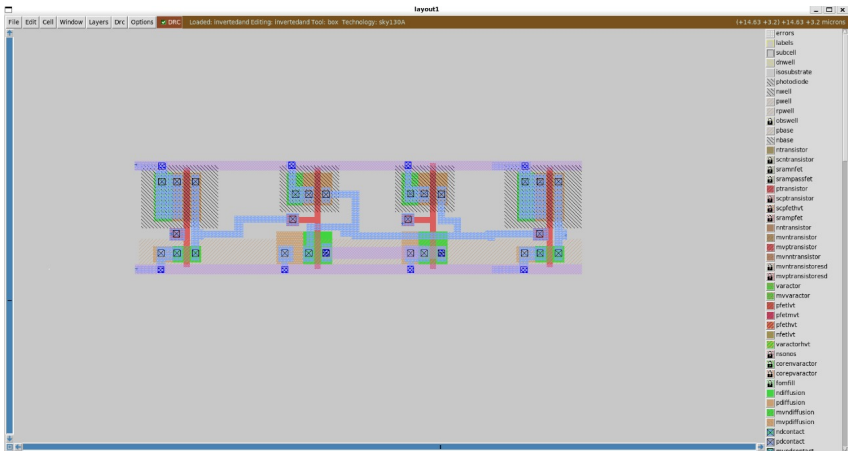

Figure 4.4: DRC clean screenshot for AND2B.

```
Contents of circuit 1:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Contents of circuit 2:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets, and 4 disconnected pins.

Circuit sky130_fd_pr__nfet_01v8 contains no devices.

Contents of circuit 1:  Circuit: 'invertedand'
Circuit invertedand contains 8 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   4
  Class: sky130_fd_pr__pfet_01v8 instances:   4
Circuit contains 40 nets.
Contents of circuit 2:  Circuit: 'invertedand'
Circuit invertedand contains 8 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   4
  Class: sky130_fd_pr__pfet_01v8 instances:   4
Circuit contains 40 nets.

Circuit 1 contains 8 devices, Circuit 2 contains 8 devices.
Circuit 1 contains 40 nets,    Circuit 2 contains 40 nets.


Final result:
Top level cell failed pin matching.

Logging to file "comp.out" disabled
LVS Done.
```

Figure 4.5: LVS clean screenshot for AND2B.

4.7 Simulation Waveforms

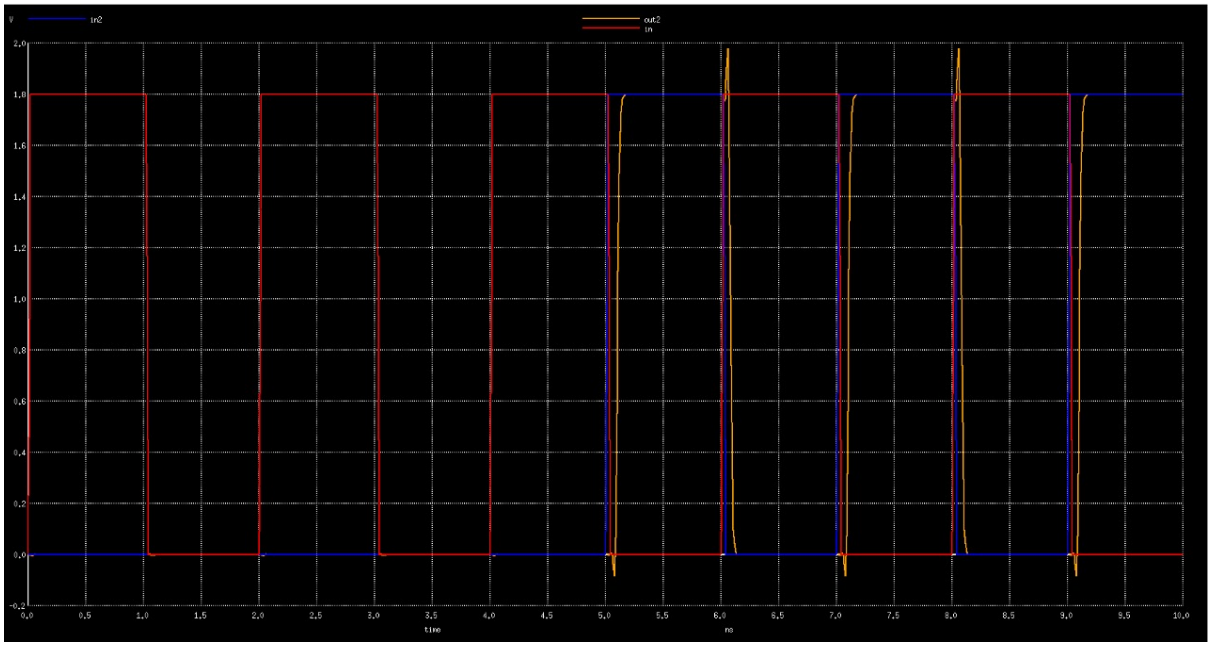

Figure 4.6: Waveform used for transition/propagation measurements (show inputs A (inverted), B and output).

4.8 Timing and Power Characterization — AND2B

subsectionInput Pin Capacitances

Table 4.2: Input pin capacitances for AND2B (pF)

Input Pin	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
A	0.00240	0.00181	0.00211
B	0.000000069	0.000000016	0.000000043

4.8.1 Transition Times

Output Rise Transitions (ns) — Related pin A

Table 4.3: Output Rise Transitions — Related pin A (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.018	0.065	0.07
100 ps	0.024	0.070	0.53
1000 ps	0.030	0.070	0.54

Output Rise Transitions (ns) — Related pin A

Table 4.4: Output Rise Transitions — Related pin A (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0157	0.0157	0.0282
100 ps	0.0687	0.0687	0.0757
1000 ps	0.5978	0.5978	0.5984

Output Rise Transitions (ns) — Related pin B

Table 4.5: Output Rise Transitions — Related pin B (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0157	0.0157	0.0282
100 ps	0.0687	0.0687	0.0757
1000 ps	0.5978	0.5978	0.5984

Output Fall Transitions (ns) — Related pin A

Table 4.6: Output Fall Transitions — Related pin A (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0195	N/A	N/A
100 ps	0.0760	0.0770	0.0842
1000 ps	0.6420	0.6420	0.6420

Output Fall Transitions (ns) — Related pin B

Table 4.7: Output Fall Transitions — Related pin B (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0195	N/A	N/A
100 ps	0.0760	0.0770	0.0842
1000 ps	0.6420	0.6420	0.6420

4.8.2 Propagation Delay Times

Cell Rise Delay (ns) — Related pin A

Table 4.8: Cell Rise Delay — Related pin A (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0546	0.0716	0.1368
100 ps	0.0973	0.1143	0.1908
1000 ps	0.4594	0.4765	0.5553

Cell Rise Delay (ns) — Related pin B

Table 4.9: Cell Rise Delay — Related pin B (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0546	0.0716	0.1368
100 ps	0.0973	0.1143	0.1908
1000 ps	0.4594	0.4765	0.5553

Cell Fall Delay (ns) — Related pin A

Table 4.10: Cell Fall Delay — Related pin A (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0864	N/A	N/A
100 ps	0.1419	0.1608	0.3126
1000 ps	0.5779	0.5975	0.7523

Cell Fall Delay (ns) — Related pin B

Table 4.11: Cell Fall Delay — Related pin B (ns)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.0864	N/A	N/A
100 ps	0.1419	0.1608	0.3126
1000 ps	0.5779	0.5975	0.7523

4.8.3 Static Power

Table 4.12: Static Power for AND2B (nW)

Condition (A1,A2,B1)	Power (nW)
000	0.187
001	0.9036
010	0.1926
011	0.9045
100	0.1872
101	0.9045
110	0.6966
111	0.0225

4.8.4 Dynamic Power

Rise Power (nW) — Related pin A

Table 4.13: Rise Power — AND2B (Related pin A)

Input Slew	Power (nW)
10 ps	234261.3
100 ps	234958.4
1000 ps	146505.7

Fall Power (nW) — Related pin A

Table 4.14: Fall Power — AND2B (Related pin A)

Input Slew	Power (nW)
10 ps	N/A
100 ps	N/A
1000 ps	N/A

Rise Power (nW) — Related pin B

Table 4.15: Rise Power — AND2B (Related pin B)

Input Slew	Power (nW)
10 ps	309644.5
100 ps	308037.1
1000 ps	298065.9

Fall Power (nW) — Related pin B

Table 4.16: Fall Power — AND2B (Related pin B)

Input Slew	Power (nW)
10 ps	32339.34
100 ps	32344.91
1000 ps	40862.82

Rise Power (nW) — Related pin (Combined)

Table 4.17: Rise Power — AND2B (Combined Summary)

Input Slew	Power (nW)
10 ps	327269.5
100 ps	327311.9
1000 ps	326301.7

Fall Power (nW) — Related pin (Combined)

Table 4.18: Fall Power — AND2B (Combined Summary)

Input Slew	Power (nW)
10 ps	3052.398
100 ps	3052.555
1000 ps	3507.169

Chapter 5

Team Contributions

Table 5.1: Contribution of Each Member

Member	Contribution
Shreesh Nagral (25M1244)	Writing the schematic for `buf` and `and2b`, layout of `buf` and `and2b`
Aryan Chaudhary (25M1251)	Writing the schematic file for `dfxtp`, layout of `dfxtp`, generating `.v` file for `and2b` and `dfxtp`, preparing circuit diagrams for the report
Abhineet Agarwal (22B1219)	Generating `.lib` file for `buf` and `and2b`, generating `.v` file for `buf`, writing the report
Manjima Karmakar (25D0522)	Layout of `dfxtp`, generating `.lib` file for `dfxtp`

Chapter 6

References

- Course Project Specification: EE671 Course Project.
- NGSpice Documentation: `http://ngspice.sourceforge.net/docs.html`
- Magic VLSI: `http://opencircuitdesign.com/magic/`
- EE-671 Lecture Notes and Slides